

CLAIMS

What is claimed is:

1. (Original) A method of exposing a bond pad comprising:
 - forming the bond pad over a silicon substrate;
 - forming a dielectric layer over the bond pad and silicon substrate;
 - forming a resist mask with at least one opening to expose the dielectric layer over the bond pad;
 - heating the resist mask with the at least one opening to form a sloped sidewall profile in the at least one opening; and
 - etching the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer, having a sloped sidewall profile and exposing the bond pad.
2. (Original) The method of claim 1 wherein the heating of the resist mask with the at least one opening persists for a time period ranging from approximately 15 seconds to approximately 90 seconds.
3. (Original) The method of claim 1 wherein the heating of the resist mask with the at least one opening is performed at a temperature ranging from approximately 160 degrees Centigrade to approximately 190 degrees Centigrade.
4. (Original) The method of claim 1 wherein the sloped sidewall profile of the at least one opening of the resist mask is wider at its upper end relative to its lower end.

5. (Original) The method of claim 1 wherein the sloped sidewall profile of the opening in the dielectric layer is wider at its upper end relative to its lower end.

6. (Original) A method of exposing a bond pad comprising:

forming the bond pad over a silicon substrate;

forming a dielectric layer over the bond pad and silicon substrate;

forming a resist mask with at least one opening to expose the dielectric layer over the bond pad;

heating the resist mask with the at least one opening to form a first sloped sidewall profile of the at least one opening; and

etching the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer that exposes the bond pad, the at least one opening in the dielectric layer further comprising a second sloped sidewall profile similar to the first sloped sidewall profile of the at least one opening of the resist mask.

7. (Original) The method of claim 6 wherein the heating of the resist mask with the at least one opening persists for a time period ranging from approximately 15 seconds to approximately 90 seconds.

8. (Original) The method of claim 6 wherein the heating of the resist mask with the at least one opening is performed at a temperature ranging from approximately 160 degrees Centigrade to approximately 190 degrees Centigrade.

9. (Original) The method of claim 6 wherein the first sloped sidewall profile of the at least one opening of the resist mask is wider at its upper end relative to its lower end.
10. (Original) The method of claim 9 wherein the first sloped sidewall profile of the at least one opening of the resist mask relative to the surface of the silicon substrate slopes at an angle of approximately 30 degrees to an angle of approximately 60 degrees.
11. (Original) The method of claim 6 wherein the forming of a resist mask with at least one opening to expose the dielectric layer over the bond pad exposes only a portion of the bond pad surface.
12. (Original) The method of claim 6 wherein the forming of a resist mask with at least one opening to expose the dielectric layer over the bond pad exposes the entirety of the bond pad surface.
13. (Original) The method of claim 6 wherein the second sloped sidewall profile of the opening in the dielectric layer is wider at its upper end relative to its lower end.
14. (Original) The method of claim 13 wherein the second sloped sidewall profile of the opening in the dielectric layer relative to the surface of the silicon substrate slopes at an angle of approximately 40 degrees to an angle of approximately 50 degrees.

15. (Original) The method of claim 13 wherein the second sloped sidewall profile of the opening in the dielectric layer has a slope sufficient to facilitate step coverage of a subsequent metallization.

16. (Original) A silicon substrate having a bond pad opening having been formed by a process comprising:

forming the bond pad over a silicon substrate;

forming a dielectric layer over the bond pad and silicon substrate;

forming a resist mask with at least one opening to expose the dielectric layer over the bond pad;

heating the resist mask with the at least one opening to form a sloped sidewall profile of the at least one opening of the resist mask; and

etching the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer having a sloped sidewall profile.

17. (Original) The sloped sidewall profile of the opening in the dielectric layer of claim 16 wherein the sloped sidewall profile of the opening in the dielectric layer is wider at its upper end relative to its lower end.

18. (Original) The sloped sidewall profile of the opening in the dielectric layer of claim 16 wherein the sloped sidewall profile of the opening in the dielectric layer relative to the surface of the silicon substrate slopes at an angle of approximately 40 degrees to an angle of approximately 50 degrees.

19. (Original) The at least one opening in the dielectric layer of claim 16 wherein the at least one opening in the dielectric layer exposes the entire bondable surface of the bond pad.

20. (Original) The at least one opening in the dielectric layer of claim 16 wherein the at least one opening in the dielectric layer exposes less than the entire bondable surface of the bond pad.

21. (Original) The bond pad opening of claim 16 wherein the bond pad opening is used to interconnect an electronic switching transistor.